REMARKS

Claims 1-2 4-7, 9, 10, 12-15 and 17-25 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

Applicants would like to thank the Examiner for the courtesy extended during the telephonic interview conducted on March 5, 2007.

DOUBLE PATENTING

Claims 1, 2, 4-7, 9, 10, 12-15 and 17-33 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-11 of copending Patent Application No. 10/626,507.

Accordingly, Applicants have attached a terminal disclaimer hereto.

CLAIM OBJECTIONS

Claims 13-15 and 17 are objected to as being substantial duplicates of claims 5-7 and 9. Applicants respectfully disagree.

For example, MPEP § 706.03(k) states that "court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways," and that "a mere difference in scope between claims has been held to be enough." Applicants respectfully note that there is at least a difference in scope between independent claims 5 and 13. For example, claim 5 does not actively claim a CPU, and instead recites a memory storage system *that is accessed by* a CPU. In other words, claim 5 is not limited by the CPU. In contrast, claim 13 recites a memory

storage system that *comprises* a first CPU. In other words, claim 13 actively claims the first CPU. As such, Applicants respectfully submit that claims 5 and 13 are different in scope and are not substantial duplicates of each other.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-2, 5-7, 10, 13-15, 18, 19 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jeddeloh (U.S. Pat. No. 7,133,972) and Loafman (U.S. Pub. Pub. No. 2005/0021916). This rejection is respectfully traversed.

With respect to claim 1, Zaidi either singly or in combination with Jeddeloh and Loafman, fail to show, teach, or suggest a line cache including a plurality of pages that are accessed by the first CPU and a first memory device that stores data that is loaded into said line cache when a miss occurs, wherein when said miss occurs and before a second miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one. Loafman appears to disclose that at least two misses occur.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, the alleged combination fails to disclose the limitation that **when said miss occurs and before a second miss occurs, n pages of said line**

cache are loaded with data from sequential locations in said first memory device, and n is greater than one.

As described in an exemplary embodiment in FIG. 24 of the present application, a **cache miss** occurs in step 504. When the cache miss occurs, n pages of line cache are loaded with data in sequential memory locations from a selected memory. In other words, the n pages of the line cache are loaded with the data from the sequential locations in response to an initial cache miss.

The Examiner acknowledges that Zaidi fails to disclose this limitation. Instead, the Examiner alleges that Loafman discloses preloading consecutive pages from lower latency storage into memory when a miss occurs in memory at Paragraph [0026]. (See Page 6, Lines 11-13 of the Office Action). The cited portion of Loafman states that a Virtual Memory Manager (VMM) 112 "anticipates future needs for pages of data of a file **by observing the pattern used by a program** that is accessing the file." (Emphasis added). More specifically, "[w]hen the program accesses two successive pages... each using a page fault, the VMM 112 assumes that the program will continue to access the data sequentially." Applicants respectfully note that a page fault occurs in response to a miss (see Paragraph [0023]). In other words, Loafman discloses retrieving the consecutive pages after observing a pattern of successive page accesses. As such, **at least two misses are required**.

During the interview, the Examiner noted that Loafman discloses that pre-fetching is known in the art. For example, Paragraph [0012] recites that "pre-fetching works splendidly when data is being read sequentially" and notes that "after two consecutive page faults of sequentially stored data, a block of sequential pages of data

will be pre-fetched." In other words, Applicants respectfully note that Loafman still discloses that the pre-fetching is only performed after two consecutive misses (i.e. page faults).

Similarly, Paragraph [0013] states:

> However, if data is being read randomly, spatial data pre-fetching may not work as well. For example, **suppose an executing program is randomly reading data. Suppose further that the executing program makes a request to read a certain amount of data that resides on two sequential pages. If the data is not already in RAM, two page faults will be raised in order to load the two pages in the RAM. Because the pages are sequential, the system may infer that data is being read sequentially; and hence, pre-fetch a block of sequential pages of data**. Since data is being read randomly, it is highly unlikely that future needed data will be on the pre-fetched block of pages. Thus, the block of pages may have been pre-fetched in vain and the physical pages onto which they are placed wasted. As will be explained later, continually pre-fetching unneeded pages of data may place an undue pressure on RAM space.

Here, Loafman discloses that when random reading of data coincidentally results in **misses of two consecutive pages**, pre-fetching may be performed. In other words, **regardless of whether data is being read randomly or sequentially, Loafman still appears to disclose that two misses are required for pre-fetching**. Loafman appears to be absent of any teaching or suggestion of loading data from sequential locations before a second cache miss.

Applicants respectfully submit that Loafman appears to be absent of any teaching or suggestion of loading multiple pages of the line cache from sequential memory locations in response to a cache miss and before a second cache miss, and instead is directed to retrieving consecutive pages after observing a pattern of (e.g. at least two) successive page accesses and multiple cache misses. Claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 5, 10, 13,

and 18, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

With further respect to claims 5 and 13, Applicants respectfully note that Loafman fails to show, teach, or suggest that after an ***initial*** miss, said line cache **prevents *any additional misses*** as long as the first CPU addresses sequential memory locations of said first memory device. As described in an exemplary embodiment in Paragraph [0091] of the present application, "[w]hen a miss occurs...instead of loading a single page of the line cache, n pages of the line cache are loaded." Further, "there will never be a miss after the initial miss." (See Paragraph [0093]).

In contrast, as best understood by Applicants, Loafman discloses that the VMM 12 assumes that the program will continue to access the data sequentially "when the program accesses two successive pages." The cited portion of Loafman appears to be absent of any teaching or suggestion of preventing **any additional misses after an initial miss** as claims 5 and 13 recite.

Applicants respectfully submit that claims 5 and 13, as well as their corresponding dependent claims, should be allowable for at least the above reasons.

Claims 4, 9, 12, 17, 26 and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jeddeloh, (U.S. Pat. No. 7,133,972 B2) and Loafman (U.S. Pub. No. 2005/0021916 A1) in further view of Barroso et al. (U.S. Pat. No. 6,725,334 B2).

Claims 4, 9, 12, 17, 26 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jeddeloh (U.S. Pat. No.

7,133,972) and Loafman (U.S. Pat. Pub. No. 2005/0021916) in further view of Alexander et al. (U.S. Pat. No. 6,131,155). These rejections are respectfully traversed.

With respect to claim 26, the alleged combinations fail to show, teach, or suggest that after a first time that said requested data is not present in said cache, n pages of said cache are loaded with data from sequential locations of one of said first and second memory devices to prevent any additional cache misses for as long as sequential memory locations of said one of said first and second memory devices are addressed.

For example, as described above with respect to claims 5 and 13, Loafman fails to disclose preventing any additional cache misses **after a first time that requested data is not present in the cache**. Instead, Loafman discloses that the VMM 112 assumes that the program will continue to access the data sequentially **after the program accesses two successive pages and multiple cache misses**. As such, Applicants respectfully submit that claim 26, as well as its dependent claims, should be allowable for at least these reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: March 5, 2007

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